

AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

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Before line 1 of the Specification, please add the following  
new paragraph:

This nonprovisional application claims priority under 35  
U.S.C. § 119(a) on Patent Application No. 091133003 filed in Taiwan  
on November 11, 2002, which is herein incorporated by reference.

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please replace the paragraph beginning on line 9 with the  
following amended paragraph:

Fig. 3a to [3p] 3o are three dimensional schematic views  
showing the manufacturing process of the mask read only memory  
containing PN diodes according to another preferred embodiment of  
the present invention, which contains three PN diode layers; and

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Please replace the paragraph beginning on line 17 with the following amended paragraph:

Fig. 3a to [3p] 3o are cross-section schematic views showing the manufacturing process of the mask read only memory containing diodes according to another preferred embodiment of the present invention.

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Please replace the paragraph beginning on line 29 with the following amended paragraph:

Next, referring to Fig. [3p] 3o, the fourth shielding layer 264 is removed to form a plurality of fifth trenches G25 along the direction B, so that the top of the fourth insulating material 274 is higher than that of the third dielectric layer 243.

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Please replace the paragraph beginning on line 4 with the following amended paragraph:

Next, still referring to Fig. [3p] 3o, a tenth conductive layer is filled into the fifth trenches G25 and planarized by CMP to form a plurality of word lines WL22. Accordingly, a mask read only memory containing diodes is accomplished, which has three layers of diodes D21, D22 and D23. As shown in Fig. [3p] 3o, the PN diode having the dielectric layer 241, 242, or 243 thereon is defined as logic "0" and the PN diode without a dielectric layer thereon is defined as logic "1". Furthermore, the word lines WL21 are commonly used by the two upper and lower layers of diodes D21 and D22, and the bit lines BL22 are commonly used by the two upper and lower layers of diodes D22 and D23.

Please replace the paragraph beginning on line 17 with the following amended paragraph:

Fig. 4 shows another mask read only memory containing diodes similar to the structure shown in Fig. [3p] 3o and having the same manufacturing method, but only comprising two layers of diodes D21 and D22. The reference numbers in Fig. 4 which are

same as those in Fig. [3p] 3o represent the same elements. As shown in Fig. 4, the mask read only memory comprises a semiconductor substrate 210; an insulating layer 212 on the semiconductor substrate 210; and two PN diode layers stacked on the insulating layer 212. Each PN diode layer comprises a plurality of vertical PN diodes and a plurality of dielectric layers disposed on part of the PN diodes. As shown in Fig. 4, the first PN diode layer comprises a plurality of vertical PN diodes D21 and a plurality of dielectric layers 241 disposed on part of the PN diodes D21, and the second PN diode layer comprises a plurality of vertical PN diodes D22 and a plurality of dielectric layers 242 disposed on part of the PN diodes D22. The reference numbers 275, 276, and 277 represent insulating material.

AMENDMENTS TO THE DRAWINGS

Attached hereto is(are) ONE (1) sheet(s) of corrected formal drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected formal drawings incorporate the following drawing changes:

FIG. 3p has been re-labeled as FIG. 3o.

It is respectfully requested that the corrected formal drawings be approved and made a part of the record of the above-identified application.